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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/039,045	12/31/2001	Hahn Vo	H052617.1142US0	2278

7590 02/26/2004

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EXAMINER	
LI, ZHUO H	
ART UNIT	**PAPER NUMBER**
2186	5

DATE MAILED: 02/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/039,045	Applicant(s) VO, HAHN	
	Examiner Zhuo H Li	Art Unit 2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13 and 16-33* is/are rejected.

7)☒ Claim(s) *14 and 15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 21-33 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 21 recites the limitation "the first memory controller " in line 8. There is insufficient antecedent basis for this limitation in the claim.

Claims 22-30 are also rejected because of depending on claim 21 containing the same deficiency.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-13 and 16-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schibinger et al. (US PAT. 6,092,156 hereinafter Schibinger) in view of Parks (US PAT. 6,356,983).

Regarding claim 1, Schibinger discloses a method of controlling access to a shared memory, i.e., memory storage unit (110, figure 1) of a multiprocessor system (100, figure 1), the multiprocessor system comprising a first bus (130A, figure 1) and a second bus (130B, figure 1) coupled to the shared memory (110A, figure 1), the first bus couple to the a first processor (120A, figure 1), and the second bus coupled to a second processor (120B, figure 1), the method comprising the steps of requesting exclusive access to a first memory location of the shared memory by the first processor, granting exclusive access to the first memory location of the shared memory to the first processor (col. 3 line 27-41 and col. 7 lines 1-39). Schibinger differs from the claimed invention in not specifically teaches the method of controlling access to a shared memory of a multiprocessor system further comprises allowing access to a second memory location of the shared memory to second processor while the first processor has exclusive access to the first memory location. However Parks teaches in the shared memory of multiprocessing system (100, figure 1) comprising a shared memory (103, figure 1) wherein the shared memory comprising a plurality of memory bank (bank0-bankm 105, figure 1), and a plurality of processor board (101, figure 1), each of the processor board is able to grant a exclusive access to any of the memory location with their unique Node ID if the request memory location indicated state is shared. In addition, Parks also teaches the when one of the processor executing it's exclusive access operation on it's requested memory address, and any other processors can able to access any other memory location with it's shared or un-cached state (col. 6 line 51 through col. 13 line 37 and table 5). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the shared memory of multiple processing system of Schibinger in having a step of allowing access to a second

memory location of the shared memory to second processor while the first processor has exclusive access to the first memory location, as per teaching of Parks, because it prevents the deadlock in the system and efficiently to minimize overheard.

Regarding claim 2, Schibinger discloses the step of requesting exclusive access comprising steps of asserting a lock signal on the first bus and send a lock request from the first processor to a memory controller coupled to the first bus, the second bus, and the shared memory (col. 6 line 23 through col. 7 line 67).

Regarding claim 3, Schibinger discloses the step of asserting a lock signal further comprising the step of asserting a split lock signal on the first bus, the split lock signal indicating that the lock request contains two memory address data (col. 8 line 17through col. 9 line 37).

Regarding claim 4, Parks discloses the step of requesting exclusive access further comprising the step of forwarding the lock request to a switch, and signaling the first processor to retry the lock request (col. 8 lines 26-36). Although Parks does not clearly teaches the lock request is forward from the memory controller to a switch, it is notoriously well know in the art that the memory is comprising a controller or a control logic to response a request from/to the requesting processor. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Parks in having a memory controller to receive a exclusive access request from the processor and forward to the switch because of increasing system efficiency.

Regarding claims 5-6, Parks discloses the step of granting exclusive access comprising steps of signaling the memory controller by the switch to retry the lock request (col. 8 lines 26-36), assigning exclusive access to the first memory location by the switch, notifying the memory

controller of the exclusive access assigned in the assigning step and granting exclusive access to the first memory location by the memory controller responsive to a retry of the lock request by the first processor, determining if the first memory location is currently assigned, saving a lock request information if the first memory location is not currently assigned and sending the lock request information to the memory controller (table 5, col. 13 line 50 through col. 14 line 16).

Regarding claims 7-8, Parks discloses the method further comprising the lock request information comprising a node ID of the first processor, a cycle ID, i.e., directory ID of the first processor and a memory address data for a first memory location (col. 6 line 51 through col. 7 line 19, figure 4 and col. 8 line 37 through col. 9 line 43).

Regarding claim 9, Parks discloses the method further comprising the step of releasing exclusive access to the first memory location (table 5 and col. 13 line 50 through col. 14 line 16).

Regarding claim 10, the limitation of the claim is rejected as the same reasons set forth in claim 1.

Regarding claim 11, Schibinger discloses the requesting step comprising asserting a lock signal on a first bus, the first bus coupling the first processor and a first memory controller (210, figure 2) of the first multiprocessor node, i.e., processing module (120, figure 1) comprising a plurality of sub-processing module (310a-310b), and sending a lock request to the first memory controller, forwarding the lock request from the first memory controller to a switch, i.e. crossbar (350, figure 3), the switch coupled to each of the plurality of multiprocessor nodes (figure 3 and col. 4 line 54 through col. 5 line 17, and col. 6 lines 3-67).

Regarding claim 12, Schibinger discloses the shared memory, i.e., memory storage unit (110A, figure 1) comprising a first memory (220, figure 2) couple to the first memory controller

(210, figure 2). Although Schibinger does not clear disclose a second memory coupled to a second memory controller for a different multiprocessor node of the plurality of multiprocessor node, it is clear the structure of the second memory (110B, figure 1) is also comprising a second memory controller and wherein the memory (110B, figure 1) is capable to access by the processing module (120b), is same as the first memory storage (110A, figure 1). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the shared memory system of multiple processing system of Schibinger in having a second memory coupled to a second memory controller for a different multiprocessor node of the plurality of multiprocessor node, because it increase the efficiently on the memory operation.

Regarding claim 13, Schibinger discloses the step of asserting a lock signal comprising the step of asserting a split lock signal on the first bus, the split lock signal indicating that the lock request contains a first memory address data and a second memory address data (col. 8 line 17through col. 9 line 37).

Regarding claim 16, the limitation of the claim is rejected as the same reasons set forth in claim 4.

Regarding claims 17-18, the limitation of the claims is rejected as the same reasons set forth in claims 5-6.

Regarding claims 19, the limitation of the claim is rejected as the same reasons set forth in claims 7-8.

Regarding claim 20, the limitation of the claim is rejected as the same reasons set forth in claim 9.

Regarding claim 21, Schibinger discloses a computer system (100, figure 1) for utilizing a shared memory, i.e.., memory storage unit (110a-110b, figure 1), the computer system comprising a first multiprocessor node (120a, figure 1), comprising a first processor bus (330A, figure 3), a first processor (310A, figure 3), couple to the first processor bus, the first processor comprising circuitry to generate an exclusive access request for a first memory location to the first memory controller (210, figure 2), a second processor bus (330B, figure 3), a second processor (310B, figure 3), coupled to the second processor bus, a first memory (220, figure 2), a first memory controller (210, figure 2) couple to the first processor bus, the second processor bus via the crossbar (350, figure 3) and the first memory (figure 2), the first memory controller adapted to perform the steps of allowing exclusive access to the first memory location by the first processor (col. 4 line 50 through col. 5 line 17, col. 3 line 27-41 and col. 7 lines 1-39). Schibinger differs from the claimed invention in not specifically teaches the second processor adapted to perform the step of requesting access to a second memory location and the first memory controller adapted to perform the step of allowing access to the second memory location by the second processor while the first processor has exclusive access to the first memory location. However, Parks teaches in the shared memory of multiprocessing system (100, figure 1) comprising a shared memory (103, figure 1) wherein the shared memory comprising a plurality of memory bank (bank0-bankm 105, figure 1), and a plurality of processor board (101, figure 1), each of the processor board is able to grant a exclusive access to any of the memory location with their unique Node ID if the request memory location indicated state is shared. In addition, Parks also teaches the when one of the processor executing it's exclusive access operation on it's requested memory address, and any other processors can able to access any other memory

location with it's shared or un-cached state (col. 6 line 51 through col. 13 line 37 and table 5). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the computer system of Schibinger in having the second processor adapted to perform the step of requesting access to a second memory location and the first memory controller adapted to perform the step of allowing access to the second memory location by the second processor while the first processor has exclusive access to the first memory location, as per teaching by the shared memory of multiple processing system of Parks, because it prevents the deadlock in the system and efficiently to minimize overheard.

Allowable Subject Matter

5. Claims 14-15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. Claims 22-33 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Buch (US PAT. 5,669,002) discloses a multiprocessor resource locking mechanism with a lock register corresponding to each resource stored in common memory (abstract).

Shagam (US PAT. 5,987,550) disclose lock mechanism for shared resources in a data processing system which each share common resources to obtain locks on those resources using a transactions which minimizes the amount of time system resources are unavailable, while also allowing system resources to be available for other processing tasks (col. 2 line 62 through col. 3 line 34).

Ramanujan (US PAT. 5,341,491) discloses apparatus and method for ensuring that lock requests are serviced in a multiprocessor system (abstract).

Chan (US PAT. 6,405,274) discloses anticipatory lock mode conversions in a lock management system (abstract).

Reuter et al. (US PAT. 6,226,717) discloses system and method for exclusive access to shared storage (abstract).

Fried et al. (US PAT. 5,142,676) discloses separate content addressable memories for storing locked segment addresses and locking processor identifications for controlling access to shared memory (abstract).

8. Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

Or faxed to:

(703) 746-7238

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Fourth Floor (Receptionist).

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zhuo H. Li whose telephone number is 703-305-3846. The examiner can normally be reached on Tuesday to Friday from 9:30 a.m. to 7:00 p.m. The examiner can also be reached on alternate Monday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim, can be reached on (703) 305-3821.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Zhuo H. Li

Art Unit 2186

MATTHEW KIM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER